Listing of Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

1. (Canceled)

2. (Currently amended) ~~A device according to claim 1~~, An integrated circuit device containing a memory area that comprises, on the one hand, a data memory and a program memory, and on the other hand, a program having N code blocks, N being an integer greater than 1,

characterized in that said memory area has M replicas, M being an integer greater than 1, of x program code blocks, x being an integer comprised between 1 and N, wherein said replicas reside at different addresses within said memory area, and in that said device comprises selection means for randomly selecting one replica of at least one of the x blocks as a block replica to be used when executing said program, and

further characterized in that the sums of bit values of at least two addresses among the set of addresses of one replicated block and its M replicas are different.

3. (Currently amended) ~~A device according to claim 1,~~ An integrated circuit device containing a memory area that comprises, on the one hand, a data memory and a program memory, and on the other hand, a program having N code blocks, N being an integer greater than 1,

characterized in that said memory area has M replicas, M being an integer greater than 1, of x program code blocks, x being an integer comprised between 1 and N, wherein said replicas reside at different addresses within said memory area, and in that said device comprises selection means for randomly selecting one replica of at least one of the x blocks as a block replica to be used when executing said program, and

further characterized in that, among the set of addresses of one replicated block and its M replicas, one address resides within the program memory and another address resides within the data memory.

4. (Currently amended) A device according to claim 3 ~~1~~, characterized in that the device ~~it~~ comprises controller means for randomly scheduling block execution.

5. (Canceled)

6. (Currently amended) ~~A method according to claim 5,~~ A method for making secure an integrated circuit device containing a memory area, which comprises, on the one hand, a data memory and a program memory, and on the other hand, a program having N code blocks, N being an integer greater than 1, characterized in that said method comprises the steps of:

generating, within said memory area, M replicas, M being an integer greater than 1, of x program code blocks, x being an integer comprised between 1 and N, wherein said replicas reside at different addresses within said memory area,

randomly selecting one replica of at lease one of the x blocks as a block replica to be used when executing said program, and

~~characterized in that said method comprises the additional step of~~ selecting the sums of bit values of at least two addresses among the set of addresses of one replicated block and its M replicas in such a way that they are different.

7. (Currently amended) ~~A method according to claim 5,~~ A method for making secure an integrated circuit device containing a memory area, which comprises, on the one hand, a data memory and a program memory, and on the other hand, a program having N code blocks, N being an integer greater than 1, characterized in that said method comprises the steps of:

generating, within said memory area, M replicas, M being an integer greater than 1, of x program code blocks, x being an integer comprised between 1 and N, wherein said replicas reside at different addresses within said memory area,

randomly selecting one replica of at lease one of the x blocks as a block replica to be used when executing said program, and

~~characterized in that,~~ among the set of addresses of a replicated block and its M replicas,

selecting an address ~~is selected~~ within the program memory and selecting another address ~~is selected~~ within the data memory.

8. (Currently amended) A method according to claim 7 ~~5~~, characterized in that said method comprises the additional step of randomly scheduling block execution.

9. (New) A device according to claim 2, characterized in that the device comprises controller means for randomly scheduling block execution.

10. (New) A method according to claim 6, characterized in that said method comprises the additional step of randomly scheduling block execution.